ENSSAT LANNION | Université de Rennes

Digital Systems Engineering for International Students

❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **French as a foreign language**
Module leader: Nathalie Caradec Nathalie.caradec@enssat.fr
Type of module: Compulsory Prerequisite: placement test for level group
Duration of module: 30 HOURS
Module components / Types of Courses: Practical courses in small group Dialogues- role play –variety of teaching material through the media and digital technology
2 ECTS
Work load: -In class studying: 30 hrs -Student managed learning: 20 hrs
Content: CEFR French levels are used on the four skills speaking – listening-reading and writing • Level A1-A2 Can introduce him/herself, can ask and answer questions about personal details such as where he/she lives, people he/ she knows, and things he/she has. Can interact in a simple way provided the other person talks slowly and clearly. • Level B1-B2 Can understand the main points of clear standard input on familiar matters regularly encountered in work, school, leisure, etc. Can deal with most situations likely to arise whilst travelling in an area where the language is spoken. Can produce simple connected text on topics which are familiar or of personal interest. Can describe experiences and events, dreams, hopes & ambitions and briefly give reasons and explanations for opinions and plans. Common European Framework of References : CECRL (Cadre Européen Commun de Références pour les Langues)
Learning outcomes: Development of the different skills according to the level.

Assessment : continuous assessment - Written assignment ☑ - Oral assignment ☑
Language of instruction: FRENCH
Additional information:

❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title : **Physical education**
Module leader: Bertrand Lefebvre bertrand.lefebvre@enssat.fr
Type of module: Compulsory
Duration of module: 30 HOURS
Course components / Types of Courses: Practical course: 30 hrs
2 ECTS
Work load: -In class studying: 30 hrs
Content: TENNIS OR WINDSURFING
Learning outcomes : - Health and safety - Team spirit - Local sport activities
Assessment - Written assignment: A final report to be handed in - Oral assignment
Language of instruction : ENGLISH/FRENCH
Additional information: swimming skills are mandatory for water sports.

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❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **English**
Module leader: Claire Le Page claire.le-page@enssat.fr
Type of module: Compulsory
Duration of module: 30 HOURS
Course components /Types of Courses: Practical courses in small groups
2 ECTS
Work load -In class studying: 30 hrs -Student managed learning: 20 hrs
Content: This course is designed to teach students at an "independent level" to communicate effectively in English at the B2 /C1 level on general topics.
Learning outcomes: At the end of this course students will be able to • Do presentations • Debate on topical issues • Interact with a degree of fluency which makes communication with a native speaker possible • Write reports on a wide range of interests • Understand the main ideas of complex texts on concrete or abstract topics • Understand extended speech or conferences
Assessment: continuous assessment - Written assignment ☑ - Oral assignment ☑
Language of instruction: ENGLISH

Additional information: B1 level is a prerequisite

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❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **Random signals and processes**
Module leader: Pascal Scalart pascal.scalart@enssat.fr
Type of module: Compulsory
Duration of module: 44 HOURS
Course components /Types of Courses: Lectures : 26 hrs, tutorials: 10 hrs, labs : 8 hrs
3 ECTS
Work load -In class studying: 44 hrs -Student managed learning : 30 hrs
Content : Course and supervised works : Introduction to random signals Continuous-time random signals Temporal law Ensemble statistics (1st, 2nd order, higher order, stationarity) Temporal moments (1st, 2nd order, higher order, ergodicity) Spectral representation of a random signal (power spectral density, polyspectra); Wiener-Khinchine theorem Examples (white noise, Gaussian, Wiener-Levy, Poissonian, SBPA processes) Linear filtering of a random signal Non-linear transformation of a random signal; Price's theorem Discrete-time random signals and estimators Sampled random signals Numerical random sequences and properties Estimation of the statistics of a random signal; estimators of the mean, the autocorrelation function, the power spectral density Labs : Time and spectral analysis of random signal realizations (Matlab simulation), practical notions of stationarity and ergodicity.
Learning outcomes : The aim is to master all the concepts required for the analysis of continuous and discrete-time random signals, in fields such as digital communications, signal and image processing, source coding and pattern recognition.
Assessment: - Written assignment

Language of instruction: ENGLISH
Additional information:

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❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **Digital Communications**
Module leader: Pascal Scalart pascal.scalart@enssat.fr
Type of module: Compulsory
Duration of module: 26 HOURS
Course components /Types of Courses: Lectures : 12 hrs, tutorials: 4 hrs, labs : 10 hrs
2 ECTS
Work load -In class studying: 26 hrs -Student managed learning : 15 hrs
Content : • Introduction to communications sytems at PHY layer: access techniques (TDMA, FDMA, WDMA, CDMA), main digital modulation techniques (base band, narrow band) • Communication channels: physical channel model (noise, attenuation, nonlinear effects, multipath channels) and communication channel model (Tx/Rx filters) • Baseband modulation: pulse shaping (NRZ, RZ, Manchester, RB, etc.); digital signal model; calculation of baseband line code power spectrum (Bennett formula) • Optimal receiver for infinite band channel: adapted filter, calculation of the binary error probability; receiver model for bandlimited channels; extension to multipolar digital signals • Narrow band digital signals: main modulation formats (ASK, PSK, FSK, QAM) • Labs: Practise and experimental study of real digital communications with baseband and several bandlimited modulations (ASK, BPSK, QPSK, BFSK, QAM-8) over different channels (bifilar, coaxial, radio, fiber optics, infrared)
Learning outcomes: • Ability to model, analyze and design basic communication systems at the physical layer • Ability to design a plan experimentation with specialized instrumentation (spectrum analyzer)
Assessment: - Written assignment
Language of instruction: ENGLISH

Additional information:

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❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **Image Processing**
Module leader: Benoit Vozel benoit.vozel@enssat.fr
Type of module: Compulsory
Duration of module: 26 HOURS
Course components /Types of Courses: Lecture: 12 hrs, tutorial: 6hrs, labs: 8 hrs
2 ECTS
Work load -In class studying: 26 hrs -Student managed learning : 15 hrs
Content: The different steps of the vision-based automatic decision making system are described: several examples of so-called "intelligent" systems are presented. After a description of the human visual system and the presentation of different image sensors, the methods and tools for improving image quality are detailed. Then, the main methods for analyzing and extracting the information content of non-textured images are developed. Finally, in order to implement the learning and identification steps, the methods of feature extraction for the characterization of objects or shapes are presented. • General introduction • Sensors • Basic tools • Image processing methods • Detection objects methods • Feature extraction
Learning outcomes: Mastery of the fundamental tools required for the design of automatic decision-making systems.
Assessment: Written assignment
Language of instruction : ENGLISH

Additional information

❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **Artificial intelligence**
Module leader: Pascal Scalart pascal.scalart@enssat.fr
Type of module: Compulsory
Duration of module: 20 HOURS
Course components /Types of Courses: Lectures : 12 hrs, tutorials: 0 hrs, labs : 8 hrs
2 ECTS
Work load -In class studying: 20 hrs -Student managed learning : 15 hrs
Content : Typology of data and learning problems, algorithmic approaches, performance evaluation, complete pipeline from sensor to use and decision and from design to production
Learning outcomes: Develop a scientific understanding of the field, measure its potential and limitations, and understand the main levers and best practices for implementation, Understand existing formalisms for representing complex data: time series, multivariate signals, relational data modeled by graphs, sequences of symbols, etc. Learn about different algorithmic approaches based on statistical, optimization or aggregation principles.
Assessment: - Written assignment: A report about the labs
Language of instruction: ENGLISH
Additional information:

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❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **Electronic Interfaces**
Module leader: Antoine Courtay Antoine.Courtay@enssat.fr
Type of module: Compulsory
Duration of module: 30 HOURS
Course components /Types of Courses: Lecture : 6 hrs, tutorial: 8hrs, lab : 16 hrs
2 ECTS
Work load -In class studying: 30 hrs -Student managed learning : 20 hrs
Content: • Microcontroller programming • Microcontroller communication interfaces • USB, UART, SPI, I2C, 1-Wire, CAN… • History, application, protocol, electrical features, use cases
Learning outcomes: This course aims to present how to communicate and exchange data with a microcontroller development board and various electronic components/devices. These components can be on the shelf components (temperature, digital potentiometer, IMU, memory card, LCD screen…) or more complex devices such as a computer or laboratory instruments (scopes, programmable power supply …). Some labs with two different platforms will explore communication standards. USB communication and driver will be the topic of one project. Then UART, SPI, I2C and 1-Wire communications will be explored with real component examples in another one.
Assessment: - Written assignment
Language of instruction: ENGLISH

Additional information

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❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **VHDL based design**
Module leader: Bertrand Le Gal bertrand.le-gal@univ-rennes.fr
Type of module: Compulsory
Duration of module: 58 HOURS
Course components /Types of Courses: Lecture : 8 hrs, tutorial : 10hrs, lab : 40 hrs
4 ECTS
Work load -In class studying: 58hrs -Student managed learning: 35hrs
Content: 1. Introduction: Why HDLs? 2. Design Flow and Tools 3. Basic Language Concepts 4. Signal and Delay Models 5. Modeling Digital Systems 6. Concurrent and Sequential Processes a Process statement, process event behavior, signals vs. variables, timing behavior of processes 7. Modeling Structures a Structural models, generics, the Generate statement 8. Simulation and Validation a Concepts, writing testbenches, configurations 9. RTL and Logic Synthesis a Writing style for logic synthesis, combinational logic, sequential logic, RTL and logic synthesis CAD algorithms 10. Fil Rouge Example: FIR filter

Learning outcomes:

The objectives of this course are to give the necessary basics about the VHDL language to be able to simulate and synthesize from the Register-Transfer Level (RTL) an application-specific integrated circuit or an FPGA. After a general introduction on hardware description languages, the design flow and execution models using HDLs are presented. The rest of the course focuses on learning the VHDL language, with first some general notions on abstractions, simulation, hardware synthesis before to present VHDL syntax and semantics following event-driven simulation of digital systems. The course ends with the presentation of the semantics following the RT level to ensure correctness by design of circuits synthesized form VHDL.

The in-class part of this course is realized using several examples that will be simulated and synthesized to illustrate the theoretical concepts. We use Mentor Graphics ModelSim for simulation and Synopsys Design Compiler for synthesis. Beyond the in-class part, this course includes a lab dedicated to logic synthesis from RTL, and a large project to design the VHDL code for a full system and to run it on an FPGA board. This project is conducted in teams of 4 to 5 students to mimic real-life design teams and to learn how to work in a team context. Examples of systems that are used in the projects are a digital oscilloscope including an FFT accelerator, a wireless CDMA emitter/receiver, a real-time audio processing system, a real-time image processing system, etc.

Assessment:

- Written assignment

Language of instruction:

ENGLISH

Additional information

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❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **VLSI Integrated Circuits and Systems: Principles and Design Method**
Module leader: Bertrand Le Gal bertrand.le-gal@univ-rennes.fr
Type of module: Compulsory
Duration of module: 26 HOURS
Course components /Types of Courses Lecture : 18 hrs, tutorial : 4 hrs, lab : 4 hrs
2 ECTS
Work load -In class studying: 26hrs -Student managed learning: 15hrs
Content • Integrated Circuit (IC) Technologies o MOS Technology, IC Fabrication, Silicon Technology Evolutions • Design of CMOS Cells o Combinatorial Logic Cells, Layout Design, Sequential Logic Cells, Delay and Power • IC Design Methods o IC Classification, Design Methods and CAD Tools, IC Specification • Synchronous Design of IC o Synchronous Design Rules and Principles, Finite State Machine (FSM) plus Datapath Model, Arithmetic Operators
Learning outcomes: The objectives of this course are to give the necessary basics in the design of application-specific integrated circuits and FPGAs. After a general introduction on the history and evolution of CMOS technology and applications, the main technologies are presented. The rest of the course focuses on CMOS circuits by presenting the main device (MOS transistor) in details. Then, transistor-level and layout-level design methods for combinatorial and sequential cells are introduced, as well as their characterization in terms of power and propagation delay. ASIC and FPGA design tools and methodologies are then presented. Finally, the last part of course focuses on synchronous design methods at logic and architecture levels. This part also includes basic notion on designing and optimizing arithmetic operators.
Assessment: - Written assignment

Language of instruction ENGLISH
Additional information

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❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **Real time systems**
Module leader: Benoît Vozel Benoit.Vozel@enssat.fr
Type of module: Compulsory
Duration of module: 36 HOURS
Course components /Types of Courses Lecture : 12 hrs, tutorial : 12hrs, lab : 12 hrs
3 ECTS
Work load -In class studying: 36 hrs -Student managed learning : 20 hrs
Content: • Basic concepts of real-time applications o Real-time applications issues • Basic concepts and illustrations for real-time task scheduling • Scheduling of independent tasks o Basic on-line algorithms for periodic tasks o Hybrid task sets scheduling o Hard aperiodic task scheduling • Scheduling of dependent tasks o Tasks with precedence relationships o Tasks sharing critical resources • Scheduling schemes for handling overload • Software environment (RT-Linux, VxWorks) • Practical study case: User requirements and functional specification, Analysis of the functional behavior, Information and control flows, Software architecture, Detailed temporal analysis

Learning outcomes :

This course encompasses the fundamental basics to real-time programming when the programmer has to design from scratch applications where a centralized computing system controls an environment (physical process to which it is connected) for controlling its behavior in real-time.

The main objectives are both to cover the fundamental basics to real-time programming and the most significant realtime scheduling policies in use today in the industry for coping with hard real-time constraints. The bases of real-time scheduling and its major variants and developments are thus described using unified terminology and notations. In addition to exercises illustrating the underlying concepts of the techniques available in the literature to solve the standard difficulties arising for hard real-time constrained systems, practical study cases with increasing complexity allow students to acquire at the output a solid approach that will then allow them to deal with real-life practical cases and implement optimized solution in complete autonomy.

Assessment:

- Written and oral assignment

Language of instruction :

ENGLISH

Additional information

❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **Real-time systems: coding**
Module leader: Emmanuel Casseau emmanuel.casseau@enssat.fr
Type of module: Elective Prerequisite: “Real time systems” module
Duration of module: 20 HOURS
Course components /Types of Courses Lab : 20 hrs
3 ECTS
Work load -In class studying: 20 h -Student managed learning: 30 hrs
Content: Real time coding of the modeling/specification of a practical application previously carried out in the “Real-time systems” module using a SART approach. The aim is to develop this application using Wind River Systems' VxWorks multitasking real-time kernel, used in many embedded systems with real-time constraints.
Learning outcomes : * Use Wind River Systems' WorkBench environment, * Understand how a multitasking real-time application works, * Understand the various inter-process communication/synchronization techniques, * Implement the most common real-time primitives (semaphores, message queues, watchdogs).
Assessment: - Project report + demo
Language of instruction: ENGLISH
Additional information Prerequisite: “Real time systems” module

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❒1st / ☑2nd/❒3rd year / Winter ❑ / Spring semester ☑

Module title: **Technical project**
Module leader: Emmanuel Casseau emmanuel.casseau@enssat.fr
Type of module: Elective
Duration of module: 10 HOURS
Course components /Types of Courses Project : 10 hrs
5 ECTS
Work load -In class studying: 10 h -Student managed learning : 60 hrs
Content Design project in electronics/embedded systems/signal processing, as a team or individually.
Learning outcomes : The project allows students to apply theoretical notions seen in class to a design project in electronics/embedded systems/signal processing, from problem definition, design, to implementation and experimentation. These projects are also the opportunity to develop written and oral communication skills.
Assessment: - Project report + oral assessment
Language of instruction: ENGLISH
Additional information